REMARKS

In the Office Action mailed January 26, 2007, Claims 1-8, 10-13 and 15-30 are rejected under 35 USC §103(a) as being unpatentable over Levi et al. (U.S. Patent 6,363,517, "Levi") in view of Miller et al. (U.S. Pub. No. 20020121913, "Miller"). Applicants have cancelled Claims 1-5 and Claims 16-20 without prejudice. Applicants reserve the right to file a divisional application to the subject matter of Claims 1-5 and 16-20 at a later time.

Applicants gratefully acknowledge the telephone conference with Applicants' representative John King and the Examiner on May 1, 2007, during which the proposed claim amendments and support for the amendments were discussed. No new matter is added by the amendments, and specific citations to Applicants' specification are provided in this response, as suggested by the Examiner, to indicate support for the amendments. Applicants appreciate the careful consideration of the proposed claim amendments by the Examiner, and believe that the claims as amended clearly distinguish over the combination of references.

Before addressing new amendments, Applicants would like to reiterate that the prior art fails to disclose elements of the claims as pending prior to the current amendments. Specifically, in response to the assertion that Levi discloses a plurality of devices having different programmable logic device architectures, Applicants respectfully submit the Levi expressly teaches away from using a plurality of devices having different programmable logic device architectures. It is suggested in the Office Action that the description of Fig. 8 in col. 13, lines 15-29 of Levi discloses systems under test having different programmable logic device architectures. However, while three FPGAs are described in col. 13, lines 15-29, there is simply no teaching or even a suggestion that these FPGAs could have different programmable logic device architectures. In contrast, Levi expressly teaches that, when an FPGA design is being evolved on several FPGAs in parallel, the various FPGAs have common architectures so they will respond the same way to the same subset of a bitstream. (Col. 11, lines 46-50). For example, evolving bitstreams for the design of a counter in an FPGA1 and an FPGA2 would require an FPGA having the same architecture according to the Levi. Assuming that the counter and the controller are implemented as a part of the same

design, the FPGA1, FPGA2 and FPGA3 would have to the same architecture. Applicants respectfully submit that Levi expressly teaches away from Applicants' claims.

However, to further distinguish Applicants' claims over the references, Applicants have amended the independent claims to indicate that each client computer generates a test job for testing a different design of a programmable logic circuit. Support for the amendments may be found at least in paragraphs [0018] and [0029]. Applicants have further amended the independent claims to indicate that the server receives a test job from a predetermined client computer. Support for the amendments may be found at least in paragraphs [0020] and [0037], and in particular step 710 of Fig. 7. As will be described in more detail below, neither reference discloses or suggests a plurality of client computers generating test jobs for testing different designs of a programmable logic circuit, or that a server receives a test job from a predetermined client computer.

In response to the newly cited Miller reference, Applicants have further amended each of the independent claims to indicate that the plurality of systems under test is shared among the plurality of client computers. Support for the amendments may be found at least in paragraph [0018]. Applicants have also amended the claims to more clearly indicate that a server is coupled to the plurality of client computers and the plurality of systems under test, and that the plurality of systems under test receives data from a predetermined client computer by way of the server. Support for the amendments may be found at least in paragraphs [0020] and [0037], and in step 710 of Fig. 7.

Finally, it is suggested in the Office Action that a plurality of client computers is disclosed by a "site host" of Miller which collects test data from individual "cell hosts." However, there is no indication that the site host is anything other than a single computer. Further, the function of the site host is to collect test data from individual cell hosts, and place compressed data in a central server. (Paragraph [0034]). Miller is directed to a "burn-in" tester applying various operating parameters, such as voltages or frequencies, in order to accelerate potential failures. In contrast to Applicants' claims which indicate that each system under test receives a test job from

a predetermined client computer by way of the server, Miller teaches that a cell host is coupled to devices under test by way of a network connection from the host cell, such as an Ethernet connection 201 as shown in Fig. 2. Because the system of Miller is used for burn-in testing, there is no need for a server between the plurality of cell hosts and the devices under test. Accordingly, Applicants respectfully submit that the claims as amended clearly distinguish over the combination of Levi and Miller. Applicants now refer to the specific language of each independent claim which distinguishes the claim over the combination of references.

Claim 6

Independent Claim 6 is directed to a client-server verification system comprising a plurality of client computers and a server. Applicants have amended independent Claim 6 to indicate that each client computer generates a test job for testing a different design of a programmable logic circuit, and that the server receives a test job from a predetermined client computer. Applicants have further amended independent Claim 6 to indicate that the plurality of systems under test is shared among the plurality of client computers by way of the server, and that each system under test of the plurality of systems under test has a programmable logic circuit which is configured with the design of the programmable logic circuit implemented according to configuration data of the test job from the predetermined client computer. Neither Levi nor Miller discloses or suggests a plurality of systems under test which are shared among the plurality of client computers by way of a server, or a plurality of client computers each having a different design, where the plurality of systems under test receive the design of the programmable logic circuit to be tested from a predetermined client computer by way of the server. Applicants submit that independent Claim 6 as amended, and its dependent Claims 7, 8 and 10, clearly distinguish over the combination of references, and respectfully request reconsideration of the claims.

Claim 21

Applicants have similarly amended the method of verifying a semiconductor design of Claim 21 to indicate that each client computer stores a test job for testing a

different design of a programmable logic circuit, where each test job has test vectors and configuration data for the different design of a programmable logic circuit. Applicants have further amended Claim 21 to indicate that each system under test of the plurality of systems under test is shared among the plurality of client computers, and is reconfigured with a design of the programmable logic circuit stored in a predetermined client computer according to configuration data of the test job coupled by way of the server. Finally, Applicants have further amended Claim 21 to indicate that corresponding test vectors of the test job for the design of a programmable logic circuit from the predetermined client computer are coupled from the predetermined client computer to each system under test by way of the test server. Neither Levi nor Miller discloses or suggests a plurality of client computers storing different designs and coupled to a plurality of systems under test, where the plurality of systems under test are configured with the design of a programmable logic circuit stored in a predetermined client computer of a plurality of client computers which share the plurality of systems under test. Further, neither Levi nor Miller discloses or suggests coupling test vectors of the test job for the design of a programmable logic circuit from the predetermined client computer to each system under test by way of the test server. Applicants have amended Claims 24 and 25 in view of the amendments to Claim 21. Applicants respectfully request reconsideration of the rejection of independent Claim 21 and dependent Claims 22-25 in view of the amendments to Claim 21.

Withdrawn Claims

Applicants respectfully request rejoinder and allowance of withdrawn Claims 11-13 and 26-30 for reasons consistent with the reasons set forth above.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 16, 2007.

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Signature